

CUSTOMER NOTIFICATION

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## **Device Files for 78K0 Series**

### **DF780547 (V2.10)**

### **User's Manual**

Be sure to read this document before using the product.

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## 1. OUTLINE

A device file is a binary file that contains device-dependent information and is prepared for each device model or for each product in the same series.

Device files are commonly used with development tools (such as assembler, compiler, and debugger). Employing device files enables generation and debugging of device-unique codes. In addition, when developing applications, device files enable the SFR names unique to the device being used to can be used for programming.

The DF780547 contains device files required for developing applications using the 78K0/KB2, 78K0/KC2, 78K0/KD2, 78K0/KE2, or 78K0/KF2 in the 78K0 Series.

## 2. CONTENTS OF PACKAGE

The device files included in this product and the corresponding devices are as follows.

**Table 2-1. Contents of Package (1/2)**

Type	Series	Device File Name	Corresponding Device Name	Pin Count	Device Specification Name	Version
Device file	KB2	DF050030.78K	μPD78F0500	30	F050030	V2.10
		DF050130.78K	μPD78F0501		F050130	V2.10
		DF050230.78K	μPD78F0502		F050230	V2.10
		DF050330.78K	μPD78F0503 μPD78F0503D		F050330	V2.10
		DF050036.78K	μPD78F0500	36	F050036	V2.10
		DF050136.78K	μPD78F0501		F050136	V2.10
		DF050236.78K	μPD78F0502		F050236	V2.10
		DF050336.78K	μPD78F0503 μPD78F0503D		F050336	V2.10
	KC2	DF051144.78K	μPD78F0511	44	F051144	V2.10
		DF051244.78K	μPD78F0512		F051244	V2.10
		DF051344.78K	μPD78F0513 μPD78F0513D		F051344	V2.10
		DF051148.78K	μPD78F0511	48	F051148	V2.10
		DF051248.78K	μPD78F0512		F051248	V2.10
		DF051348.78K	μPD78F0513		F051348	V2.10
		DF051448.78K	μPD78F0514		F051448	V2.10
		DF051548.78K	μPD78F0515 μPD78F0515D		F051548	V2.10

Type	Series	Device File Name	Corresponding Device Name	Pin Count	Device Specification Name	Version
Device file	KD2	DF052152.78K	μPD78F0521	52	F052152	V2.10
		DF052252.78K	μPD78F0522		F052252	V2.10
		DF052352.78K	μPD78F0523		F052352	V2.10
		DF052452.78K	μPD78F0524		F052452	V2.10
		DF052552.78K	μPD78F0525		F052552	V2.10
		DF052652.78K	μPD78F0526		F052652	V2.10
		DF052752.78K	μPD78F0527 μPD78F0527D		F052752	V2.10
	KE2	DF053264.78K	μPD78F0532	64	F053264	V2.10
		DF053364.78K	μPD78F0533		F053364	V2.10
		DF053464.78K	μPD78F0534		F053464	V2.10
		DF053564.78K	μPD78F0535		F053564	V2.10
		DF053664.78K	μPD78F0536		F053664	V2.10
		DF053764.78K	μPD78F0537 μPD78F0537D		F053764	V2.10
	KF2	DF054480.78K	μPD78F0544	80	F054480	V2.10
		DF054580.78K	μPD78F0545		F054580	V2.10
		DF054680.78K	μPD78F0546		F054680	V2.10
		DF054780.78K	μPD78F0547 μPD78F0547D		F054780	V2.10

The device file name and device specification name are determined as shown below.

Pin count

Product name

The user environment for device files depends on the environment for the development tools to be used.

#### 4. CORRESPONDING VERSIONS OF DEVELOPMENT TOOLS

The corresponding versions of the DF780547 and 78K0 Series development tools made by NEC Electronics are shown below. Use these tools in the following combinations.

**Table 4-1. Corresponding Versions of Development Tools**

Tool Used	Version of Corresponding Tool
C compiler package CC78K0	V3.70 or later
Assembler package RA78K0	V3.80 or later
Integrated debugger ID78K0-QB	V2.90 or later
USB Driver	V1.10 or later
Project manager PM plus	V5.21
System simulator SM+ for 78K0/Kx2	SM780547-B V1.01 or later

**Remark** When using the DF780547 with the QB-78K0KX2, use the QB-78K0KX2 with control code D or later.

#### 5. INSTALLATION

Install the device file with the following procedure.

- (1) Download the device file from the NEC Electronics website (Development Tools Download webpage) to any folder.  
<http://www.necel.com/micro/ods/eng/index.html> (English version)  
<http://www.necel.com/micro/ods/jpn/index.html> (Japanese version)
- (2) Double-click the downloaded file and choose a folder where the files are to be saved; the downloaded file is then decompressed.
- (3) Start the device file installer<sup>Note 1</sup> from the Start menu<sup>Note 2</sup>.
- (4) Click the [Install] button.
- (5) Click the [Browse] button to specify the directory where the decompressed files are located. If installing from the floppy disk, insert the floppy disk in the host machine then click the [FD Browse] button.
- (6) The *Necsetup.ini* file and *\_csetup.ini* file are displayed in the file list of the dialog box that appears after step (5). Selecting which file depends on the language of the OS used.  
 Open *\_csetup.ini* (English version)  
 Open *Necsetup.ini* (Japanese version)
- (7) Follow the installation wizard to continue installation.

- Notes**
1. The device file installer is automatically installed when an NEC Electronics development tool (CC78K0, RA78K0, ID78K0-QB, or SM+ for 78K0/Kx2 (under development)) is installed.
  2. The device file installer is registered under "NECTools32" in the Start menu. To directly start the execution file, start "DFINST.EXE" which exists under the directory "*installation directory*\NECTools32\bin".

## 6. USAGE

Refer to the user's manual of each tool for details on how to use the device file.

## 7. DEFAULT LINK DIRECTIVE INFORMATION

Each device has different ROM and RAM capacities. The assembler package has default link directive information necessary to relocate the user's program and data in the device file according to the ROM capacity and RAM capacity of each product.

In order to change the setting of the default, the user should create a link directive for each target system according to the memory configuration of the actual target system using the assembler package (linker). Note that user's program, data, and stack may not be appropriately located in the default link directive information. This means, for example, that user's data and stack may be located overlapping the register bank area and the reserved area of the C compiler.

The default link directive information depends on the device as shown below.

The area name ROM and RAM are essential area names. All the code segments (CSEG) are relocated in the area name ROM area and all the data segments (DSEG) and bit segments (BSEG) are relocated in the area name RAM area unless otherwise specified explicitly in the MERGE statement.

**Table 7-1. Default Link Directive Information (1/2)**

Device	Default Link Directive Information
$\mu$ PD78F0500	MEMORY ROM: (00000H, 02000H) MEMORY RAM: (0FD00H, 00300H)
$\mu$ PD78F0501 $\mu$ PD78F0511 $\mu$ PD78F0521 $\mu$ PD78F0531	MEMORY ROM: (00000H, 04000H) MEMORY RAM: (0FC00H, 00400H)
$\mu$ PD78F0502 $\mu$ PD78F0512 $\mu$ PD78F0522 $\mu$ PD78F0532	MEMORY ROM: (00000H, 06000H) MEMORY RAM: (0FB00H, 00500H)
$\mu$ PD78F0503 $\mu$ PD78F0513 $\mu$ PD78F0523 $\mu$ PD78F0533 $\mu$ PD78F0503D $\mu$ PD78F0513D	MEMORY ROM: (00000H, 08000H) MEMORY RAM: (0FB00H, 00500H)
$\mu$ PD78F0514 $\mu$ PD78F0524 $\mu$ PD78F0534	MEMORY ROM: (00000H, 0C000H) MEMORY IXRAM: (0F400H, 00400H) MEMORY RAM: (0FB00H, 00500H)
$\mu$ PD78F0515 $\mu$ PD78F0525 $\mu$ PD78F0535 $\mu$ PD78F0515D	MEMORY ROM: (00000H, 0F000H) MEMORY IXRAM: (0F000H, 00800H) MEMORY RAM: (0FB00H, 00500H)

**Table 7-1. Default Link Directive Information (2/2)**

Device	Default Link Directive Information
$\mu$ PD78F0526 $\mu$ PD78F0536	MEMORY ROM: (00000H, 08000H) MEMORY BANK0: (08000H, 04000H) MEMORY IXXRAM: (0E800H, 01000H) MEMORY RAM: (0FB00H, 00500H) MEMORY BANK1: (18000H, 04000H) MEMORY BANK2: (28000H, 04000H) MEMORY BANK3: (38000H, 04000H)
$\mu$ PD78F0527 $\mu$ PD78F0537 $\mu$ PD78F0527D $\mu$ PD78F0537D	MEMORY ROM: (00000H, 08000H) MEMORY BANK0: (08000H, 04000H) MEMORY IXXRAM: (0E000H, 01800H) MEMORY RAM: (0FB00H, 00500H) MEMORY BANK1: (18000H, 04000H) MEMORY BANK2: (28000H, 04000H) MEMORY BANK3: (38000H, 04000H) MEMORY BANK4: (48000H, 04000H) MEMORY BANK5: (58000H, 04000H)
$\mu$ PD78F0544	MEMORY ROM: (00000H, 0C000H) MEMORY IXXRAM: (0F400H, 00400H) MEMORY LRAM: (0FA00H, 00020H) MEMORY RAM: (0FB00H, 00500H)
$\mu$ PD78F0545	MEMORY ROM: (00000H, 0F000H) MEMORY IXXRAM: (0F000H, 00800H) MEMORY LRAM: (0FA00H, 00020H) MEMORY RAM: (0FB00H, 00500H)
$\mu$ PD78F0546	MEMORY ROM: (00000H, 08000H) MEMORY BANK0: (08000H, 04000H) MEMORY IXXRAM: (0E800H, 01000H) MEMORY LRAM: (0FA00H, 00020H) MEMORY RAM: (0FB00H, 00500H) MEMORY BANK1: (18000H, 04000H) MEMORY BANK2: (28000H, 04000H) MEMORY BANK3: (38000H, 04000H)
$\mu$ PD78F0547 $\mu$ PD78F0547D	MEMORY ROM: (00000H, 08000H) MEMORY BANK0: (08000H, 04000H) MEMORY IXXRAM: (0E000H, 01800H) MEMORY LRAM: (0FA00H, 00020H) MEMORY RAM: (0FB00H, 00500H) MEMORY BANK1: (18000H, 04000H) MEMORY BANK2: (28000H, 04000H) MEMORY BANK3: (38000H, 04000H) MEMORY BANK4: (48000H, 04000H) MEMORY BANK5: (58000H, 04000H)

In the above table, area RAM includes the SFR area (0FF00H to 0FFFFH). Note that, however, since the linker handles the SFR area as a reserved area, the segments (user's data and stack) are not relocated in this area. For example, the result for "MEMORY RAM: (0FB00H, 00500H)" and "MEMORY RAM: (0FB00H, 00400H)" is the same.

## 8. REVISIONS FROM V2.00 TO V2.10

The following points have been changed from DF780547 V2.00 to V2.10.

- Device files for  $\mu$ PD78F0500,  $\mu$ PD78F0501,  $\mu$ PD78F0502,  $\mu$ PD78F0503, and  $\mu$ PD78F0503D 36-pin packages have been added.
- Specification changes for the option byte are now supported.

## 9. REVISION HISTORY

**Table 9-1. Revision History**

Document Number	Issued on	Description
ZUD-CD-05-0009	September 7, 2005	1st edition